21. The method of claim 13 further including the step, between said steps (e) and (f), of:

growing a gate oxide about the silicon region in said vias.

Remarks

The above Amendments and these Remarks are in reply to the Office Action mailed June 19, 2002.

Claims 1-21 were pending in the Application prior to the outstanding Office Action. In the Office Action, the Examiner has withdrawn claims 1-12 from consideration, objected to the drawings, disclosure, abstract, and claims, and rejected claims 13-21. The present Response amends claims 17-19, leaving for the Examiner's present consideration claims 13-21. No new matter has been added by the amendments made in this response. Reconsideration of the objections and rejections is requested.

Objections to Drawings

The drawings were objected to as failing to comply with 37 CFR 1.84(p)(5) because they did not include reference signs mentioned in the description (page 1, reference signs 10, 12, 14, 16; page 10, reference signs 120a, 120b), they included reference signs not mentioned in the description (reference sign 236, FIG. 14c), and a reference sign appeared to indicate one element in the figures and a different element in the specification (reference sign 230 as a material layer in FIG. 14b, as an opening in page 8).

Figures 1, 4B, 5B, 13A, 14A-14C, 15A-15C, and 16A have been amended in response to this objection. In particular, Figures 1, 4B and 5B were amended to include reference signs mentioned in the specification but not indicated in the figures, Figures 13A, 14A, 15A and 16A were amended to correct typographical errors, and Figures 14B, 14C, 15B and 15C were amended to clarify these figures with respect to the specification. Figures 14B, 14C, 15B and 15C were amended to clarify that element 230 is intended to be a see-through-view of an opening.

Applicant respectfully submits that the amended drawings are now in position to overcome the objections to the drawings, and respectfully requests these rejections be withdrawn.

Objection to the Abstract

The Examiner has objected to the Abstract because it contains more than 150 words. Applicant has amended the Abstract to contain less than 150 words. Applicant respectfully submits the amended Abstract is now in position to overcome this objection, and respectfully requests the objection be withdrawn.

Objection to the Disclosure

The Examiner has objected to the disclosure because of a typographical error at page 10, line 10, and the description of concentrations in page 10. Application has amended the specification to correct the typographical error and the description of the concentrations in page 10. No new matter has been added by these amendments. Applicant respectfully submits the amended disclosure is now in position to overcome this objection, and respectfully requests the objection be withdrawn.

Objection to the Claims

The Examiner has objected to claims 17-19 because of the notation in the claims used to describe a concentration. Applicant has amended claims 17-19 to correct the notation used to describe a concentration as indicated by the Examiner. Applicant respectfully submits the amended disclosure is now in position to overcome this objection, and respectfully requests the objection be withdrawn.

Rejection to the Claims under 35 USC §112

Examiner has rejected claims 13-21 under 35 USC §112 as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art at the time the application was filed that the inventor had possession of the claimed invention. In particular, the Examiner states that the specification does not disclose exposing a portion of the silicon region by removing a portion of the first nitride mask, as recited in step (e) of claim 13. Applicant respectfully traverses this rejection.

The specification as amended discloses "a directional etch of the TEOS 210 and the first nitride layer opens two vias 240, 245 in the substrate, as well as removing the first nitride over the polysilicon 122, exposing the underlying silicon 122", at page 12, lines 13-16. Applicant respectfully submits that this portion of the disclosure discloses the cited portion of step (e) in claim 13. The amendment to the specification involved changing the TEOS reference from 220 to 210 and the underlying silicon reference from 140 to 122. Both of these changes were typographical errors. No new matter was added by these amendments to the specification.

Applicant respectfully submits that the claims are now in condition to overcome the 35 USC §112 rejection and requests the rejection be withdrawn.

Conclusion

In light of the above, it is respectfully submitted that all of the claims now pending in the subject patent application should be allowable, and a Notice of Allowance is requested. The Examiner is respectfully requested to telephone the undersigned if he can assist in any way in expediting issuance of a patent.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: September 13, 2002

By: _____

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APPENDIX

In the Specification:

Page 10, line 10 through Page 11, line 2:

As shown in Figure 9B, a source/drain/gate impurity implant is then performed to form the source and drain regions of the device of the present invention. The implant is such that the nitride 150 covering the channel area prevents implantation of the impurity into the channel region. Depending on the device size and strength of the impurity implant, the nitride 110 may be supplanted by an additional layer of oxide formed between nitride 110 and second nitride 155.

For an N-channel device, arsenic or phosphorous may be deposited to a concentration of approximately 2-4x10^{15}/cm^3 [cm^2] at energies of approximately 15-20 KeV (arsenic) or 7-10 KeV (phosphorous). For a P-channel device, boron may be implanted into a concentration of 2-3x10^{15}/cm^3 [cm^2]at energies of approximately 1.5-2.5 KeV. Zero degree tilt implants are used for these embodiments. The implants are then subsequently annealed in a rapid thermal anneal for approximately 5-10 minutes at a temperature of 1000-1025°C.

Page 12, lines 13-22:

Next, as shown in Figures 15A-15C, a directional etch of the TEOS 210[220] and the first nitride layer opens two vias 240,245 in the substrate, as well as removing the first nitride over the polysilicon 122, exposing the underlying silicon 122[140]. Following via formation, a gate oxide 242 may be grown by immersing the structure in an oxygen-containing atmosphere for two minutes. Following gate oxide growth, a polysilicon fill 250 forms the three-sided gate region 200 out of silicon overlying the silicon island 122. The polysilicon deposition may be in-situ doped with a desired impurity concentration to form the three sided gate structure 200 surrounding island 122.

In the Abstract:

A self-aligned transistor and method making a self-aligned transistor, the transistor including a first silicon portion on an isolation layer, the silicon portion having formed therein a source region and a drain region separated by a channel region. The channel region has a first side and a second side and a top portion, and a gate oxide surrounds the channel on said first side, second side and top portion. A first, a second and a third silicon gate regions are positioned in a second silicon portion surrounding the first silicon portion about the first side, second side and top portion and the channel region.

[Also disclosed is a method for manufacturing a transistor device. The method for manufacturing includes the steps of: providing a substrate having a buried oxide region; depositing a first nitride mask layer having a pattern overlying a silicon region; forming a trench in said substrate with a depth to said buried oxide; depositing a conformal oxide in said trench; forming vias in said conformal oxide adjacent to said silicon region and removing a portion of said first nitride mask to expose a portion of said silicon region; depositing polysilicon in said vias and on said portion of said silicon region; and implanting an impurity into exposed portions of polysilicon in said trench and of said silicon-on-insulator substrate underlying said second nitride layer.]

In the Claims:

17. The method of claim 13 wherein said step (f) comprises implanting arsenic at an energy of 15-20 KeV with a zero degree tilt to provide a concentration of 2-4x$10^{15}/cm^3$[1015/cm-2].

18. The method of claim 13 wherein said step (f) comprises depositing phosphorous at an energy of 7-10 KeV with a zero degree tilt to provide a concentration of the impurity in a range of 2-4x$10^{15}/cm^3$[1015/cm-2].

19. The method of claim 13 wherein said step (f) comprises depositing boron at an energy of 1.5-2.5 KeV with a zero degree tilt to provide a concentration of the impurity in a range of 2-3x$10^{15}/cm^3$[1015/cm-2].